REMARKS

Applicant respectfully requests reconsideration of this application. Claims 1-36 are pending. No claims have been amended, cancelled, or added.

Therefore, claims 1-36 are now presented for examination.

Claim Rejection under 35 U.S.C. §102

Lin, et al.

The Examiner rejected claims 1-2, 4-6, 8-11, 13-14, 16-17, 19-21, 23-26, 28-29 and 35-36 under 35 U.S.C. § 102 (b) as being anticipated by U.S Patent 6,421,798 of Lin, et al. (hereinafter referred to as "*Lin*").

While the arguments provided in the prior response remain valid are hereby restated, the Applicant will focus on the response to arguments provided in the Final Office Action. **The Applicant will demonstrate that not only are elements of the claims missing from the *Lin* reference, it is impossible logically and physically for these elements to be applied to the system described in *Lin*.**

For the convenience of the Examiner, claim 1 is again provided here:

1. A circuit comprising:
   a first device coupled with a first bus, wherein the first device is not compliant with a standard, the first device containing data, wherein the data is not operational for the circuit with a device that is not compliant with the standard;
   a second device coupled with a second bus, wherein the second device is compliant with the standard, the second device to be associated with the data from the first device, the association of the second device with the data from the first

device enabling the data from the first device to be utilized according to the standard; and

a memory to receive the data from the first device.

Thus, claim 1 provides for a first device coupled with a first bus, with the first device not being compliant with a standard, and a second device coupled with a second bus, with the second device being compliant with the standard. Claim 1 also provides that "the data is not operational for the circuit with a device that is not compliant with the standard", and "the second device to be associated with the data from the first device, the association of the second device with the data from the first device enabling the data from the first device to be utilized according to the standard". (emphasis added) It is again submitted that, in addition to other differences, that *Lin* does not provide for data that is not operational for the circuit with a device that is not compliant with a standard to be associated with a second device that is compliant with the standard, with the association of the second device with the data from the first device enabling the data to be utilized according to the standard.

In response to the argument presented by the Applicant, the Final Office Action indicates the following:

> *Lin* clearly discloses a first device [figure 3, element 104 – system BIOS] coupled with a first bus [figure 3. element 330 – ISA bus] and a second device [figure 3, element 114] coupled with a second bus [figure 3, element 308 – PCI bus], wherein the first device is not compliant with a standard [system BIOS is ISA compliant] and the second device is compliant with the standard [test card 114 is PCI compliant] and associating the second device with the data from the first device so that the data can be utilized according to the standard [column 6, lines 24-34 – to enable caching of the portion of high-speed BIOS code (i.e., 'the data'), a

loader routine in the enhanced BIOS code causes the high-speed to be loaded into cache memory by first writing it into memory locations associated with a high-speed address space of PCI address space – meaning the code from the BIOS is associated with the PCI protocol in order to allow the PCI device to utilized the code/data.]

It is respectfully submitted that the response provided in the Final Office Action does not contain an accurate description of Claim 1 in at least two essential respects. First, the Examiner has not addressed the element of claim 1 indicating that the **data contained in the first device** (which is coupled with a first bus and which is not compliant with a standard) **is not operational for the circuit with a device that is not compliant with the standard.** In addition, the Final Office Action refers to "associating the second device with the data from the first device so that the data can be utilized according to the standard". This not what the claim indicates. The claim provides "the second device to be associated with the data from the first device, the association of the second device with the data from the first device enabling the data from the first device to be utilized according to the standard". It is submitted that *Lin* does not address either of these elements.

As discussed in the prior response, *Lin* relates to chipset-based memory testing for hot-pluggable memory, and is intended to provide a method for a computer system to test physical memory devices. The system is divided into two separate areas of address space, with one or more physical memory devices being associated with a first area of system address space. The system is operated from the second area of system address space, allowing the memory locations associated with the first area of the system address space to be tested, the one or more tested physical memory devices to be replaced with

untested physical memory devices without dropping power to the system, and then testing the replacement devices by repeating the test cycle. The system thus operates without interruptions when replacing the physical memory devices for testing. (See, e.g., *Lin*, col. 2, lines 16-30)

Within this system, there is a **system BIOS** (*Lin*, Fig. 3, element 104, which is flash ROM) coupled with an **ISA bus** (*Lin*, Fig. 3, element 330), and a **PCI test card** (*Lin*, Fig. 3, element 114) coupled with a **PCI bus** (*Lin*, Fig. 3, element 308).

In this structure, *Lin* provides that: "The disclosed system is distinguishable from the prior art in that the BIOS code has been modified such that after start-up, the PCI card 114 enables the memory power switch 116 to drop power only to the physical memory 108 such that it may be pulled from its memory slot 10 and replaced while the computer system is running, precluding the need to power down the system to replace the memory for testing. This is accomplished by not running the system BIOS code from the physical memory 108, but from PCI memory space using a coordinated effort of the system BIOS 104, cache memory 106, and the PCI card 114, which will be discussed in greater detail hereinbelow." (*Lin*, col. 3, line 59 to col. 4, line 3) (emphasis added) Thus, in order to enable the memory testing method, the system BIOS is not run from physical memory, but from PCI memory space.

However, there is no data identified in the reference that is not operational with a device that is not compliant with a standard, as provided in claim 1. The identified first device is the **System BIOS ROM**, which contains the **BIOS for the computer system**. The standard that the Final Office Action has identified is **the PCI bus** to which the **PCI card** 114 is attached (the second device, as identified by the Final Office Action). In

order for these elements to relate to the elements of claim 1, the Final Office Action must then be arguing that the BIOS is not operational for the circuit with a device that is not compliant with a PCI bus. This is impossible both logically and physically. First, in normal operation, the BIOS must be operational when attached to the ISA bus, and in fact the BIOS boots from the BIOS flash ROM. The BIOS data MUST BE operational for the circuit with a device that is not compliant with the PCI bus or the computer system could not boot up. Thus, the position taken by the Final Office Action is not logically possible. Second, it is emphasized the data is the system BIOS itself – it would not appear to make any sense for the physical operation of the computer system for the BIOS data to be limited to the PCI bus, as the argument provided in the Final Office Action must require in order to provide the elements of claim 1. Thus, it is not possible for *Lin* to provide the described element of claim 1.

With regard to the second element, there is no teaching or suggestion that the association of the BIOS data with the PCI test card enables the BIOS code from the first device to be utilized according to the PCI standard. The point of *Lin* is to provide a method for testing memory in a PC, replacing the tested memory with new untested memory, and then testing the new untested memory while the PC is operational. In order to accomplish this intent, what *Lin* does is to not run "the system BIOS code from the physical memory 108, but from PCI memory space using a coordinated effort of the system BIOS 104, cache memory 106, and the PCI card ..." (*Lin*, col. 3, line 66 to col. 4, line 2) The association of the BIOS code with the PCI card does not enable the BIOS to be utilized according the PCI standard – rather, the BIOS is in fact booted from the BIOS ROM, and is run from the PCI memory space to avoid the physical memory. The BIOS

is being run from PCI memory space in order to drop the power to the physical memory so that it can be pulled from the slot and replace. (*Lin*, col. 3, lines 59-66) Thus, the association of the BIOS data with the PCI test card does not enable the BIOS code from the BIOS ROM to be utilized according to the PCI standard.

Thus, it is respectfully submitted that all elements of claim 1 are not provided by *Lin*, as require for a rejection of the claim under 35 U.S.C. § 102 (b). Further, it is submitted that the application of the claim elements to the system provided in *Lin* is logically and physically impossible.

For this reason, the rejection of claim 1 under 35 U.S.C. § 102 (b) must be removed.

It is submitted the above argument also applies to the other independent claims, as amended herein, claims 9, 16, and 24. The remaining claims are dependent claims and are allowable as being dependent on the allowable base claims.

Claim Rejection under 35 U.S.C. §103

Lin, et al. in view of Powderly, et al.

The Examiner rejected claim 22 under 35 U.S.C. § 103 (a) as being unpatentable over *Lin* as applied to claim 16 in view of U.S. Patent Number 6,560,641 of Powderly, et al. (hereinafter referred to as "*Powderly*").

In addition to any other differences, the rejected claim is allowable as being dependent on the allowable base claim, as indicated above. *Powderly*, which relates to emulation or remote control of a console of a host computer from another computer remotely located on a network, does not teach or suggest the elements of the claims missing from *Lin*.

Claim Rejection under 35 U.S.C. §103

Lin, et al. in view of Ma

The Examiner rejected claims 3, 12, 18, 27, and 31-34 under 35 U.S.C. § 103 (a) as being unpatentable over Lin and further in view of U.S Patent Publication 2004/0003297 of Ma (hereinafter referred to as "*Ma*").

In addition to any other differences, the rejected claims are allowable as being dependent on the allowable base claims, as indicated above. *Ma*, which describes an apparatus for PCI power management intended to allow the system to conditionally enable or disable PCI power management, does not teach or suggest the elements of the claims missing from *Lin*.

Conclusion

Applicant respectfully submits that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the claims as amended be allowed.

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (503) 439-8778 if there remains any issue with allowance of the case.

Request for an Extension of Time

The Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action should one be required. Please charge our Deposit Account No. 02-2666 for the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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